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TITLE OF INVENTION: UNIVERSAL MODULATOR

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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [x] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [x] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [x] is attached hereto (required only if not communicated by the International Bureau).
   b. [ ] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [ ] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [ ] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [x] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [x] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [x] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [x] Other items or information:
    Eight (8) sheets of drawings, in triplicate; copy of the International Publication with Search Report; copy of the International Preliminary Examination Report; copy of the Written Opinion; copy of the Reply to Written Opinion; and Application Data Sheet

UNIVERSAL MODULATOR

BACKGROUND

The present invention generally relates to cable television (CATV) and consumer video communication systems. More particularly, the invention relates to a dual-conversion universal modulator having programmable synthesized phase-locked loop oscillators driving their respective mixers which select a specific HI-IF frequency depending upon what output frequencies or standards are desired. Such standards include NTSC, PAL, NICAM, DIN, SECAM and any other known standard.

To allow reception of more than the 12 VHF channels on an older television receiver, most CATV systems require a settop terminal at a subscriber's location. Today, settop terminals not only provide a means for accepting a plurality of channels broadcast with varying bandwidths and guardbands for forward and reverse frequencies, but they also secure pay television services from unauthorized viewing. Other functions include decoding digital video and audio, interactive services, creating personalized viewer channels and the like.

In addition to the conversion from a cable transmission to a standard output frequency, a variety of descrambling techniques are employed depending upon the techniques used at a system headend. CATV equipment manufacturers are developing more sophisticated scrambling techniques using complicated encryption methods and digital processing to thwart pirating.

Most settop terminals are tunable. A block diagram for a prior art settop terminal is shown in **Figure 1**. Incoming signals from a CATV transmission network are coupled to an input bandpass amplifier and up-converted to a high intermediate frequency (HI-IF). The up-conversion requires a tunable local oscillator which selects a desired channel and an associated mixer. The mixer is coupled to a bandpass filter and down-converted to an IF channel using a fixed-frequency local oscillator and mixer. The output channel is filtered and forwarded to a subscriber's television receiver. Prior art settop terminals use one down-converter mixer with an oscillator having slight frequency agility to provide an output at one or two preselected channel frequencies. The output frequencies and bandwidths depend upon the transmission standard used.

In the United States, the NTSC (National Television System Committee) is the standard for color television. Other countries have chosen different systems. SECAM (*sequentiel couleur avec mémoire*) is used by France and Russia. PAL A and PAL B (phase alternation line) are used by many European countries such as Germany and the United Kingdom. Accordingly, television receivers are typically manufactured for a specific transmission standard. For worldwide use, a settop terminal must be adapted to the established broadcast standards.

U.S. Patent No. 5,640,697 teaches the use of two predetermined frequencies for each local oscillator, whereby the second oscillator frequency can be adjusted independently of the first oscillator frequency. Adjustment between the two

frequencies is used to adapt to the different output frequencies, while eliminating noise caused by the local oscillators. Similar to U.S. Patent No. 5,640,497, German Patent No. Application 4,306,578 adjusts the oscillator frequencies by a predetermined amount in order to eliminate noise. PCT International Patent Application No. 84/04637 employs two local oscillators that generate predetermined frequencies, in which the second oscillator is selected between one of two frequencies to eliminate this noise.

Accordingly, there exists a need for an inexpensive method to adapt the output of a settop terminal to a variety of television broadcast standards.

SUMMARY

The present invention is a universal modulator that accepts baseband audio and video inputs and modulated audio or data and converts the combined signal to one of a plurality of frequencies in dependence upon a desired output frequency and broadcast standard. The universal modulator is located between baseband video and audio outputs of a settop terminal demodulator/decoder and an antenna input of a television receiver or other audio/video component (such as a VCR). The universal modulator includes a dual conversion architecture using an up-converter mixer and a down-converter mixer. Each mixer receives an oscillator input from a corresponding addressable, programmable, PLL (phase-locked loop) frequency synthesizer. Each PLL frequency is controlled by firmware in the settop terminal. Configuration is performed via manual input using settop terminal controls, or interrogation directly by the CATV headend or by programmed settings. A communication bus coupled to the firmware distributes addressable instructions to selectively control each PLL frequency and obviate oscillator difference beat frequencies (ODBFs) that may be manifested.

Accordingly, it is an object of the present invention to provide a universal modulator within a settop terminal which is able to couple a CATV transmission network to a customer's television receiver notwithstanding the broadcast standard used to transmit the television programs.

Other objects and advantages will become apparent to those skilled in this art after reading the detailed description of the preferred embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a prior art CATV settop terminal.

Figure 2 is a block diagram of a settop terminal incorporating the present invention.

Figure 3 is a block diagram of the preferred embodiment of the universal modulator of the present invention for use in a settop terminal.

Figure 4 is a block diagram of an addressable, programmable, phase-locked loop.

Figure 5 is a flow chart of the universal modulator configuring process.

Figure 6 is a flow chart of the ODBF translation process.

Figure 7 is a block diagram of a prior art headend.

Figure 8 is a block diagram of a headend made in accordance with the present invention.

Figures 9A and 9B are graphs of oscillator difference beat frequencies.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiment will be described with reference to the drawing figures where like numerals represent like elements throughout.

Figure 2 is a block diagram of a settop terminal **17** with the universal modulator **19** shown coupled to the output of a demodulator/decoder **21**. The demodulator/decoder **21** outputs a customer's channel selection as baseband audio **23** and video **25**. The functional description of the demodulator/decoder **21** is beyond the scope of the present invention **19** and shall not be described. An alternate audio source **27**, such as a NICAM carrier or modulated audio, may also be supplied and output **29**.

The higher quality baseband audio **23** and video **25** signals are available as settop terminal outputs **31**, **33** and may be coupled to television receivers that have baseband inputs. For television receivers that lack this feature, the universal modulator **19** provides an up-conversion output **35** compatible with the television broadcast standard used, from baseband to VHF or UHF for coupling to an antenna input.

The demodulator/decoder **17** outputs baseband audio **23** and video **25** and an alternate audio carrier **27** which differs from the baseband audio output. A reference clock signal **37** originating from a master oscillator and a common communication bus **39** are also coupled to the modulator **19**.

The universal modulator **19** is shown in more detail in **Figure 3**. The common communication bus **39** shown is an I^2C interface from Phillips® Electronics. Other bus communication protocols may alternatively be used. The configuration for a settop terminal **17** may be downloaded from the CATV system headend via a dedicated channel, or inband on the VBI of a channel. One skilled in this art would

appreciate that an advanced cable system can address and interrogate a specific settop terminal and alter its functionality. If the settop terminal has all configurations stored in firmware, the CATV system headend may simply instruct the settop terminal **17** of the standard being used. In this fashion, the settop terminal **17** does not require a technician to configure the unit but can auto-configure upon initial energization.

The communication bus protocol permits configuring component parameters to a particular broadcast standard using a unique addressing system within the settop terminal **17**. As shown in **Figure 3**, the I^2C bus **39** communicates with: a baseband audio programmable PLL frequency synthesizer **41**, a second audio carrier switched input **43**, adjustable amplifiers for the baseband video input **45** and baseband audio input **47**, a programmable PLL frequency synthesizer **49** for an up-converter mixer **91** and a programmable PLL frequency synthesizer **51** for a down-converter mixer **101**. Although third addressable programmable PLL **51** has been described as being coupled to a "down-converter" mixer **101**, the down-converter mixer **101** may in fact further up-convert the HI-IF signal to a higher frequency signal. It should be noted that each PLL frequency synthesizer **41**, **49**, **51** has an associated oscillator driver **L01**, **L02**, **L03** respectively (not shown). Each respective component has its own address to permit firmware contained parameters to be loaded for a given broadcast standard configuration.

The alternate audio input **53**, modulated by the demodulator/decoder **21**, is coupled to the solid state switch **43**. The output of the switch **43** is coupled to a first input **55** of a summing amplifier **57**. The baseband video input **59** is coupled to a clamp **61** which limits signal amplitude. The output from the clamp **61** is coupled to the video adjustable amplifier **45** where signal gain is increased or attenuated depending upon the broadcast standard. The output from the adjustable amplifier **45** is coupled to a hard limiter **63** which clips signal peaks. The output from the limiter **63** is coupled to a second input **65** of the summing amplifier **57**. The baseband audio input **67** is coupled to a baseband audio mixer **69** via an adjustable amplifier **68**. The baseband audio mixer **69** modulates the baseband to the broadcast standard. The baseband audio mixer **69** may be selectively activated or deactivated by the I^2C bus as required to support the standard in use. The output from the baseband audio mixer **69** is coupled to a lowpass filter **71** to remove RF. A second input to the audio lowpass filter **71** is provided as a modulated audio input **72**. The audio lowpass filter **71** is coupled to an audio adjustable amplifier **47** where signal gain is increased or attenuated. The audio adjustable amplifier **47** output is coupled to a third input **73** of the summing amplifier **57**.

Each of the mixers mix a signal input with the outputs of the three addressable, programmable PLL frequency synthesizers **41**, **49**, **51**. The PLL output frequencies vary depending on the broadcast standard and the RF output

frequency **105** desired. An addressable, programmable PLL frequency synthesizer **41, 49, 51** is shown in **Figure 4**.

The PLL **41, 49, 51** includes a phase detector **75**, a voltage-controlled oscillator (VCO) **77** and a loop filter **79**. The programmable PLL uses digital and analog techniques for frequency synthesis. The phase detector **75** compares two input frequencies **81a, 81b** and generates an output **83** that is a measure of their phase difference. If both inputs **81a, 81b** differ in frequency, the output is periodic at the difference frequency. If the frequency input does not equal the frequency output of the VCO **77**, the phase-error signal, after being filtered, causes the VCO frequency to deviate in the direction of the input frequency. When the frequencies match, the VCO **77** locks to the input frequency maintaining a fixed phase relationship with the input signal. The filtered output of the phase detector **75** is a dc signal. A modulo-*n* counter **87** is coupled between the VCO **77** output and the second input **81a** to the phase detector **75** to generate a multiple of the input reference frequency providing frequency synthesis.

Each PLL synthesizer **41, 49, 51** employed in the present invention **19** is addressable such that the input frequency can be adjusted by using an input modulo-*n* counter **89** or divide-by-*n* to adjust output frequency. Both the input frequency divide-by-*n* **89** and loop frequency divide-by-*n* **87** are addressable components. Each of the PLLs **41, 49, 51** are addressed and controlled in accordance with a predetermined

settop terminal **17** configuration. The configuration determines both the output frequency and operating bandwidth of the settop terminal **17** and adjusts the up- and down-converter PLLs **49, 51** accordingly.

Referring back to **Figure 3**, the summer amplifier **57** output is modulated with the frequency output from the second programmable PLL **49** to drive the up-conversion modulator **91** and translate the summed output to a high intermediate frequency (HI-IF) **93**. The HI-IF **93** is higher than the highest expected frequency in the summed amplifier **57** output bandwidth. In the present invention **19**, the input to the up-converter mixer **91** is not bandwidth limited.

The summing amplifier **57** output frequencies are translated to a new bandwidth, starting at a low frequency of the second PLL **49** minus the highest input band frequency, and ending at a high frequency of the third PLL **51** minus the lowest input band frequency. The second PLL **49** frequency is selected to translate the summing amplifier **57** output to correspond to the passband of an intermediate lowpass filter **95**. The output from the lowpass filter **95** is coupled to a buffer amplifier **97** to restore gain losses. The output from the buffer amplifier **97** is input to a final lowpass filter **99**. The buffer amplifier **97** maintains the system noise figure by overcoming the losses in the up-conversion mixer **91** and first HI-IF filter **95**. The signal is filtered by a HI-FI filter **99,** with the output coupled to a down-conversion mixer **101**. The third PLL synthesizer **51** is coupled to the down-conversion mixer **101**. The difference between the HI-IF **93**

and the third PLL **51** frequency is the desired output channel in the IF band. It should, however, be noted that the down-converter mixer **101** may accept the HI-IF **93** and further up-convert the signal to a higher frequency RF signal. The output is then filtered via a low pass filter **103**, (or other appropriate filter if up-converted), and forwarded as an RF output frequency **105** for reception by a television receiver.

As discussed above, the second **49** and third **51** programmable PLLs are controlled by the common communication bus **39**. The bus **39** is coupled to a processor in the settop terminal demodulator/decoder **21** which receives instructions from the system headend or from the settop terminal's **17** keypad. The configuration takes place transparently upon initial energization of the unit **17** if the system headend is equipped to send broadcast configuration instructions to the settop terminal **17**. If the system headend does not have this capability, the settop terminal **17** is configured via the keypad and function display (not shown). The configuration request, whether from the headend or at a consumer location, outputs the predetermined parameters onto the I^2C bus **39** for each of the addressable components. The predetermined parameters are related to the standard that is being employed by the CATV system on which the settop terminal **17** is located. These parameters will include the determination of whether a second audio carrier **53** exists, whether the baseband audio input **67** or the modulated audio input **72** are to be used and the frequency at which the RF output frequency **105** is desired. These parameters may also include any other

configurable parameters which are employed by any of the addressable components coupled to the communication bus **39**. It should also be recognized that since many of the components are addressable by the communication bus **39**, a user may manually input and address a particular component and selectively configure that component if desired.

An undesirable artifact of dual conversion is the generation of harmonics based on the fundamental oscillator frequencies. The harmonics of the second and third PLL frequency synthesizers **49, 51** mix with each other, thereby creating ODBFs. To obviate the intrusive effects of these PLL harmonics, the system and method of the present invention **19** eliminate this type of interference by translating the significant ODBFs out of the desired output channel.

A flowchart of the preferred method of the present invention **19** is shown in **Figure 5**. Upon making the necessary connections to the CATV cable **15** and subscriber's television receiver, the settop terminal **17** is energized **(step 201)** establishing communication with the system headend. If the cable system headend has forward communication ability **(step 205)**, the settop terminal is instructed how to configure itself for the applicable broadcast standard by downloading the parameters for the regional standards being used and the channel broadcast maps **(step 207)**. The predetermined PLL frequencies derived from the channel and broadcast maps in memory are converted into corresponding "divide-by" numbers for the PLL modulo-*n* converters **87, 89** and output to the second **49** and third **51** PLL frequency synthesizers. The

settop terminal **17** acknowledges when configuration is complete. If the cable system does not have forward communication capability, the user will be prompted to enter the applicable information via a display and keypad, thereby manually loading the applicable broadcast configuration **(step 209)**.

The settop terminal **19** reviews the loaded channel and broadcast maps. The predetermined frequencies are examined for potential ODBFs **(step 211)**. If it is determined that ODBF's are likely **(step 213)**, an ODBF translation is performed **(step 215)** as shown in **Figure 6** (which will be explained in greater detail hereafter). Otherwise, the original frequencies are maintained **(step 217)** (**Figure 5**). The frequencies are addressed to their respective PLL synthesizers as words over the I^2C communication bus **(step 219)**.

Referring to the flow diagram of **Figure 6**, the elimination of ODBFs is achieved by selectively adjusting the frequencies of the second **49** and third PLLs **51** to obtain the desired RF output frequency. For a typical NTSC signal, the up-converter mixer **91** modulates the input video **59** and audio signals **67** with the output **93** of the second PLL **49** to up-convert the input RF signal of the selected channel to the HI-IF **93 (step 301)**.

$$LO1 = \text{audio carrier frequency} \qquad \textbf{(Equation 1)}$$

$$LO2 = \text{HI-IF} \qquad \textbf{(Equation 2)}$$

The down-converter mixer mixes **101** the HI-IF **93** with the output of the third PLL synthesizer **51 (step 303)** to down-convert, (or further up-convert if desired), to obtain the desired RF output frequency **105.**

$$LO3 = (HI - IF) + RF\ output \qquad \textbf{(Equation 3)}$$

Multiples of the second and third PLL synthesizer **49, 51** fundamental frequencies define the even and odd harmonics,

$$m(LO2)\ and\ m(LO3),\ for\ m = 1, 2, 3, 4, \ldots \infty, \qquad \textbf{(Equation 4)}$$

which represent all possible harmonics **(step 305).** However, due to the high system frequencies involved, examination of frequencies beyond the 10th harmonic is unnecessary.

The existence of an interfering ODBF is determined by serially calculating the differences between two harmonics of the second **49** and **51** third PLL synthesizers that are separated by at least one degree until the absolute value of an $ODBFm,n$ is within a given bandwidth or a predetermined number of $ODBFm,n$ values are calculated. When an $ODBFm,n$ absolute value is found within the RF channel bandwidth, it is designated as an interfering oscillator difference beat frequency (ODBF). The general equation for calculating ODBFs is:

$$OBDF_{m,n} = (m + n)\ (LO2) - (m)(LO3),\ for\ m = 1, 2, 3, 4, \ldots 10,$$

(Equation 5)

with $n = 1$ for a first series, $n = 2$ for a second series, $n = 3$ for a third series, and so on up to $n = 8$ for all previously calculated harmonics **(step 305)**. The $ODBFm,n$ calculated from the differing degrees of the second **49** and third PLL **51** harmonics are then examined **(step 307)**. For example, if the ODBF lies outside of the desired RF output channel bandwidth, no adjustment of the second **49** and third **51** PLL frequency synthesizers is required.

For an ODBF which falls inband, the following equations can be used to determine which direction the second **49** and third **51** PLL frequencies should be adjusted to translate the ODBF out of band. In these equations, CLB is the channel low-band; CMB is the channel mid-band; and CHB is the channel high-band.

If -CHB≤ODBF<-CMB; then HI-IF is moved downward. **(Equation 6A)**

(If the result of **Equation 5** is negative and the magnitude is greater than the mid-band of the desired RF output channel **(step 309)**, the HI-IF is moved downward **(step 311)**).

If -CMB≤ODBF≤-CLB; then HI-IF is moved upward. **(Equation 6B)**

(If the result of **Equation 5** is negative and the magnitude is less than or equal to the mid-band of the desired RF output channel **(step 313)**, the HI-IF is moved upward **(step 315)**).

If CLB≤ODBF≤CMB; then HI-IF is moved downward. **(Equation 6C)**

(If the result of **Equation 5** is positive and the magnitude is less or equal to than the mid-band of the desired RF output channel **(step 317)**, the HI-IF is moved downward **(step 319)**).

If CMB<ODBF≤CHB; then HI-IF is moved upward. **(Equation 6D)**

(If the result of **Equation 5** is positive and the magnitude is greater than the mid-band of the desired RF output channel **(step 321)**, the HI-IF is moved upward **(step 323)**).

The second **49** and third **51** PLLs are then adjusted **(step 327)** in accordance with the following: To translate the oscillator difference beats below or above the desired RF output channel, the following equation is used to determine the Δ in

frequency for the second **49** and third **51** PLL frequency synthesizers.

$$\Delta = \frac{CMB - [(m+n)(LO2) - m(LO3)]}{(m+n) - m} \quad \textbf{(Equation 7)}$$

The new second **49** and third **51** PLL frequencies (LO2' and LO3' respectively) are derived as shown in LO2' is calculated as shown in **Figure 6**.

The new PLL frequencies LO2' and LO3' translate the ODBFs above or below the desired RF output channel. The new PLL frequency values are used to program the second **49** and third **51** PLL frequency synthesizers **(step 327)**.

In an alternative embodiment, a fixed value for Δ can be used to simplify the calculations and the operation of the system. For example, a value of 4 MHz for Δ will suffice for NTSC and PAL systems.

The present invention will now be explained with reference to several examples. In the first example, if the HI-IF is 960 MHz and the desired RF output channel has a picture carrier frequency of 319.25 MHz, we have the following:

LO2 = HI-IF = 960 MHz; and **(from Equation 2)**

LO3 = HI-IF + RF output **(from Equation 3)**

= 960 + 319.25 = 1279.25 MHz.

The graph for ODBFs versus the RF output frequencies for m=2 and n=1 is shown in **Figure 9A**. If m=2 and n=1, then:

$$ODBF_{2,1}(960) = (m+n)(LO2) - m(LO3) \quad \textbf{(from Equation 5)}$$
$$= 3(960) - 2(1279.25)$$
$$= 2880 - 2558.5 = 321.5 \text{ MHz}$$

Since the desired RF output channel has a picture carrier frequency of 319.25 MHz (and assuming the bandwidth is 6 MHz for an NTSC channel), the ODBF is in-band for the desired RF output channel. From **Equation 6D**, since the ODBF is above the mid-band of the desired RF output channel, the HI-IF is moved upward. Assuming that Δ will be a fixed value of 4 MHz, LO2' will be 964 MHz and LO3' will be 1283.25 MHz. Accordingly, from **Equation 5**:

$$ODBF_{2,1}(964) = 3(964) - 2(964+319.25)$$
$$= 2892 - 2566.5 = 325.5 \text{ MHz}$$

The ODBF is now out of band.

In the second example, if the HI-IF is 960 MHz and the desired RF output channel has a picture carrier frequency of 481.25 MHz, we then have the following:

$$LO2 = \text{HI-IF} = 960 \text{ MHz; and} \quad \textbf{(from Equation 2)}$$

$$LO3 = \text{HI-IF} + \text{RF output} \quad \textbf{(from Equation 3)}$$
$$= 960 + 481.25 = 1441.25 \text{ MHz.}$$

The graph for ODBFs versus the RF output frequencies for m=3 and n=1 is shown in **Figure 9B**. If m=3 and n=1, the ODBF can be calculated as:

$$ODBF_{3,1}(960) = 4(960)-3(1441.25) \quad \textbf{(from Equation 5)}$$
$$= 3840-4323.75$$
$$= -483.75MHz.$$

Since the selected channel is 481.25 MHz, (and assuming an NTSC channel), the ODBF is in-band and the HI-IF must be relocated. The result of **Equation 5** for this example is negative and the magnitude is greater than the mid-band of the desired RF output channel (481.25 MHz). Accordingly, from **Equation 6A**, the HI-IF is moved lower. Assuming that Δ will be a fixed value of 4 MHz, LO2' will be 956 MHz and LO3' will be 1437.25 MHz. Recalculating the ODBF provides:

$$ODBF_{3,1}(956) = 4(956)-3(956+481.25) \quad \textbf{(from Equation 5)}$$
$$= 3824-4311.75 = -487.75 \text{ MHz}.$$

The ODBF is now out of band.

Due to the simple design of the present invention and since there are no shielding requirements to avoid ODBFs, the universal modulator may be incorporated onto a single integrated circuit. This was not possible with prior art signs.

Although the present invention has been described with reference to a settop terminal, it should be understood by

those of skill in the art that the invention is adaptable to other applications within the CATV environment, or even other communication applications which do not pertain to CATV systems.

For example, as shown in **Figure 7**, a prior art headend **700** generally includes two pieces of equipment; a baseband section **702** and an IF section **704**. These two sections **702**, **704** are typically designed to operate as "stand alone" units. Together, the two sections **702**, **704** output a single RF channel. The baseband section **702** generally comprises a video section **706** and an audio section **708**. These sections **706**, **708** receive audio and video baseband inputs and combine these inputs to an intermediate frequency for output to the IF section **704**. In the IF section **704**, the intermediate frequency is up-converted to the desired RF output channel. Since both sections **702**, **704** comprise units of equipment which are designed to work independently, this requires the duplication of many components between units **702**, **704**.

Referring to **Figure 8**, a headend **800** made in accordance with the present invention is shown. The headend **800** includes an audio pre-processing section **802**, a video pre-processing section **804**, the universal modulator **808** of the present invention (which is coupled to two filters **810**, **812**), a transmitter **814** (if desired), and a microprocessor **806**, which controls all of the components of the headend **800**. As was previously described hereinbefore, since the universal modulator **808** can convert a baseband input signal to any desired RF output signal while avoiding ODBFs, the universal

modulator **808** may be utilized to replace most of the components in the baseband section **702** and the IF section **704**. This significantly reduces the number of components required for a headend **800**. Accordingly, the cost and complexity are also thereby reduced.

It should be understood by those of skill in the art, with reference to **Figure 8**, that the universal modulator **808** of the present invention may also be used to accept a baseband digital VSB signal and remodulate the signal to a desired RF output signal for use with broadcast HDTV television receivers. The universal modulator **808** could also be used to transmit RF signals to devices which require high frequency RF signals, including wireless appliances such as a cordless telephone or a wireless LAN receiver. In such an application, the second mixer up-converts the HI-IF signal to a higher frequency RF signal, instead of down-converting the HI-IF as previously described. The desired RF output signal would be:

$$\text{RF output} = (\text{HI-IF}) + \text{LO3} \qquad \textbf{(Equation 10)}$$

The RF output signal may then be transmitted directly to the wireless appliance.

* * *

WE CLAIM:

1. A communication module which receives an input RF signal and converts said input RF signal to a desired RF output signal (105), the communication module comprising:

a first frequency agile local oscillator (49) for generating a first frequency for mixing with said input RF signal to generate a high intermediate frequency (HI-IF) signal;

a second frequency agile local oscillator (51) for generating a second frequency for mixing with said HI-IF signal to generate said desired RF output signal (105);

a processor including:

a controller for controlling said first and second frequency agile local oscillators (49, 51) to obtain said desired RF output signal (105); and

a comparator for comparing said first frequency with said second frequency to determine whether any interfering oscillator difference beat frequencies (ODBFs) exist within the bandwidth of said desired RF output signal (105), and for calculating a delta value to avoid said ODBFs; whereby said processor adjusts said first and second frequency agile local oscillators by said delta value such that said first and second frequencies move said interfering ODBFs outside the bandwidth of said desired RF output signal (105).

2. The communication module of claim 1 wherein the communication module receives a plurality of input RF signals and said communication module further includes a signal selector for

selecting one of said plurality of input RF signals for mixing with said first frequency.

3. The communication module of claim 1 further comprising a transmitter, for wirelessly transmitting said RF output signal (105) to a receiver.

4. The communication module of claim 3, whereby said transmitted signal is transmitted within the UHF or VHF frequency bands.

5. The communication module of claim 1, whereby the communication module is encompassed within a single integrated circuit.

6. The communication module of claim 1, whereby the communication module comprises an RF receiver circuit.

7. The communication module of claim 1, whereby the communication module comprises an RF transmitter circuit.

8. The communication module of claim 1 wherein said selected signal represents an analog signal transmission.

9. The communication module of claim 1 wherein said selected signal represents a digital signal transmission.

10. The communication module of claim 2 wherein said processor further comprises collateral memory for storing a channel map of channels to predetermined channel carrier frequencies; whereby said processor receives a specific channel selection request and determines said initial first local oscillator frequency.

11. A universal modulator for receiving a plurality of baseband input signals and outputting a desired RF output signal (105) comprising:

a first PLL frequency synthesizer (41) for generating a first frequency for mixing with a baseband audio signal to relocate said baseband audio signal within a desired bandwidth;

a second PLL frequency synthesizer (49) for generating a second frequency for mixing with a summed signal within the desired bandwidth which includes said relocated baseband audio signal and a baseband video signal to produce a HI-IF signal;

a third PLL frequency synthesizer (51) for generating a third frequency for mixing with said HI-IF signal to produce an RF output signal (105); and

a processor for selecting said first (41), second (49) and third (51) PLL frequency synthesizers based upon said desired RF output signal (105) whereby said processor:

determines a first PLL frequency for said first synthesizer (41);

determines a second initial PLL frequency for said second synthesizer (49);

compares said second initial PLL frequency with a third initial PLL frequency for said third synthesizer (51) to determine whether any interfering oscillator difference beat frequencies exist within the bandwidth of said RF output signal (105); and

adjusts said second and third initial PLL frequencies to move any interfering ODBFs out of the bandwidth of said RF output signal (105).

12. A method for receiving an input RF signal and converting said input RF signal to a desired RF output signal (105), the method comprising:

generating a first frequency for mixing with said input RF signal to generate a high intermediate frequency (HI-IF) signal;

generating a second frequency for mixing with said HI-IF signal to generate said desired RF output signal (105);

controlling said first and second frequency agile local oscillators to obtain said desired RF output signal (105);

comparing said first frequency with said second frequency to determine whether any interfering oscillator difference beat frequencies (ODBFs) exist within the bandwidth of said desired RF output signal (105), and for calculating a delta value to avoid said ODBFs; and

adjusting said first and second frequency agile local oscillators by said delta value such that said first and second frequencies move said interfering ODBFs outside the bandwidth of said desired RF output signal.

said interfering ODBFs outside the bandwidth of said desired RF output signal.

ABSTRACT

A universal modulator that accepts baseband audio and video inputs and converts the combined signal to one of a plurality of frequencies dependening upon a desired output frequency and broadcast standard. The universal modulator is coupled between baseband video and audio outputs of a settop terminal demodulator/decoder and an input of a television receiver. Configuration of the universal modulator is performed via manual input by settop terminal controls or interrogation directly by a CATV headend. A communication bus coupled to the firmware distributes addressable instructions to selectively control addressable PLL frequency synthesizers. The modulator also obviates oscillator difference beat frequencies that may manifest themselves since programmable PLL frequency synthesizers are used.

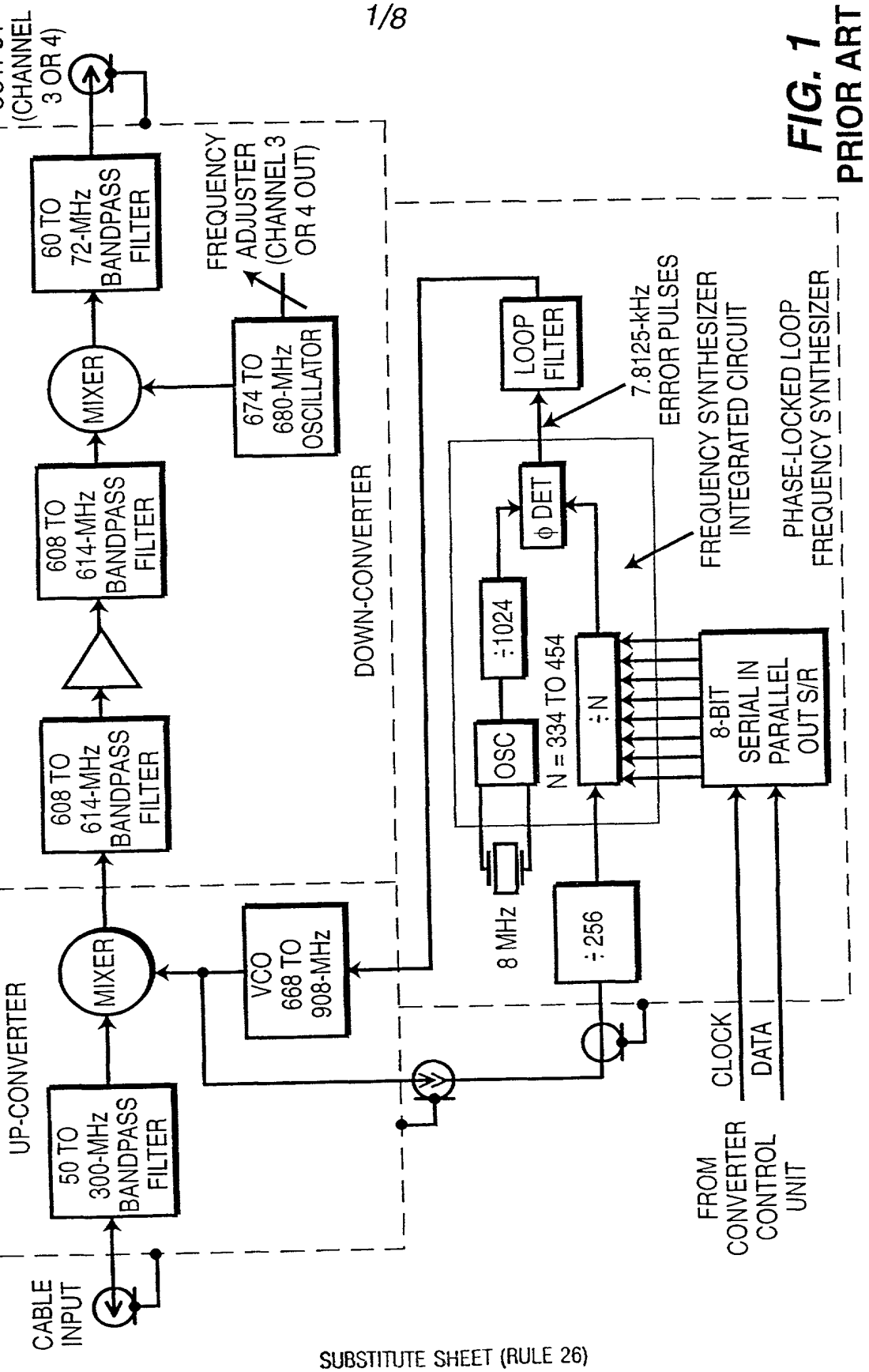

FIG. 1
PRIOR ART

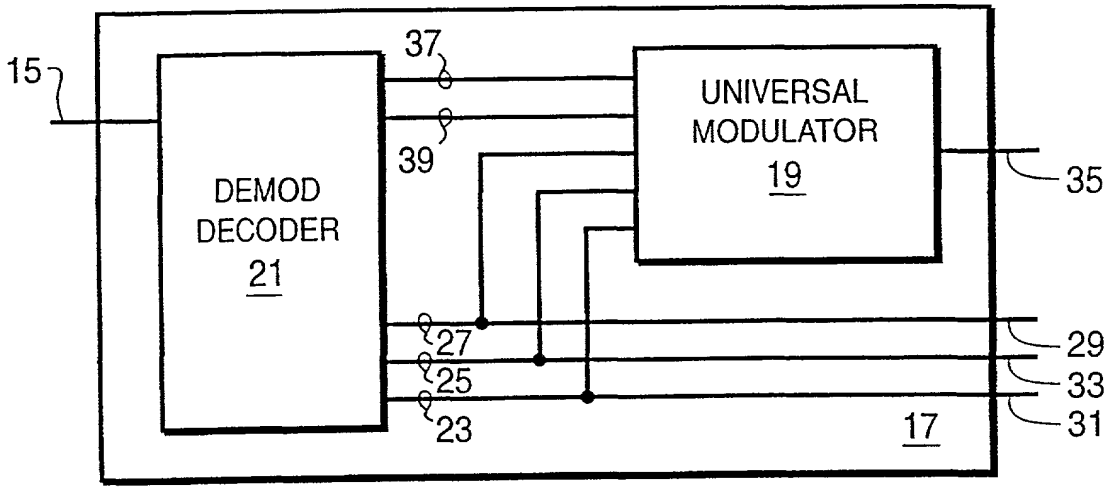
15
37
39
DEMOD
DECODER
21
UNIVERSAL
MODULATOR
19
35
27
25
23
29
33
31
17

FIG. 2

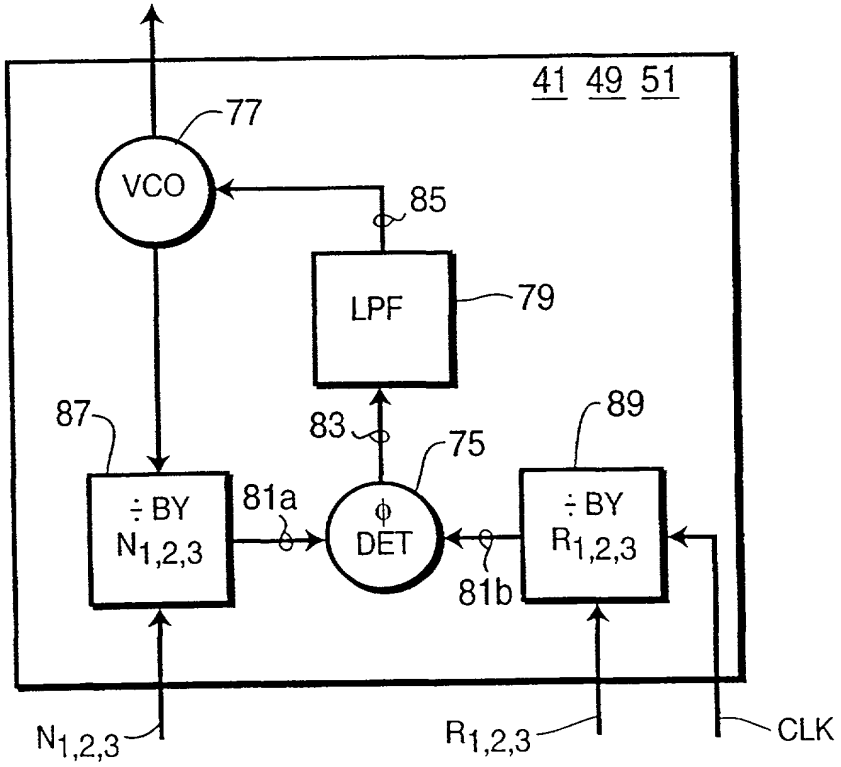
41 49 51
77
VCO
85
LPF
79
87
83
75
89
÷ BY
N1,2,3
81a
φ
DET
÷ BY
R1,2,3
81b
N1,2,3
R1,2,3
CLK

FIG. 4

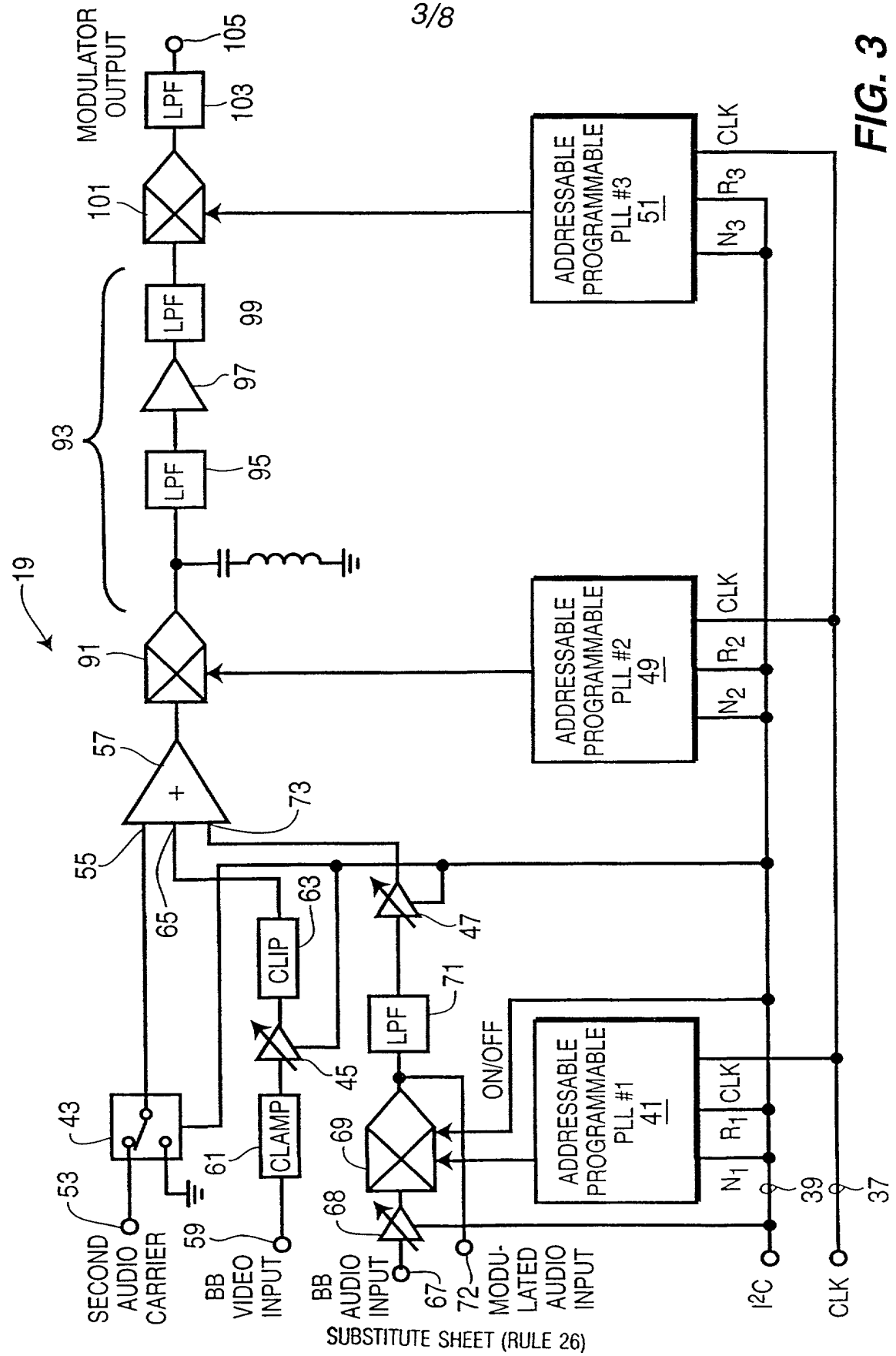
MODULATOR OUTPUT
105
LPF
103
101
LPF
99
97
93
LPF
95
19
91
57
+
73
55
65
63
CLIP
47
71
LPF
45
ON/OFF
43
61
CLAMP
69
68
53
59
67
72
SECOND AUDIO CARRIER
BB VIDEO INPUT
BB AUDIO INPUT
MODU-LATED AUDIO INPUT
ADDRESSABLE PROGRAMMABLE PLL #3 51
ADDRESSABLE PROGRAMMABLE PLL #2 49
ADDRESSABLE PROGRAMMABLE PLL #1 41
CLK
R_3
N_3
R_2
N_2
R_1
N_1
39
37
I^2C
CLK

FIG. 3

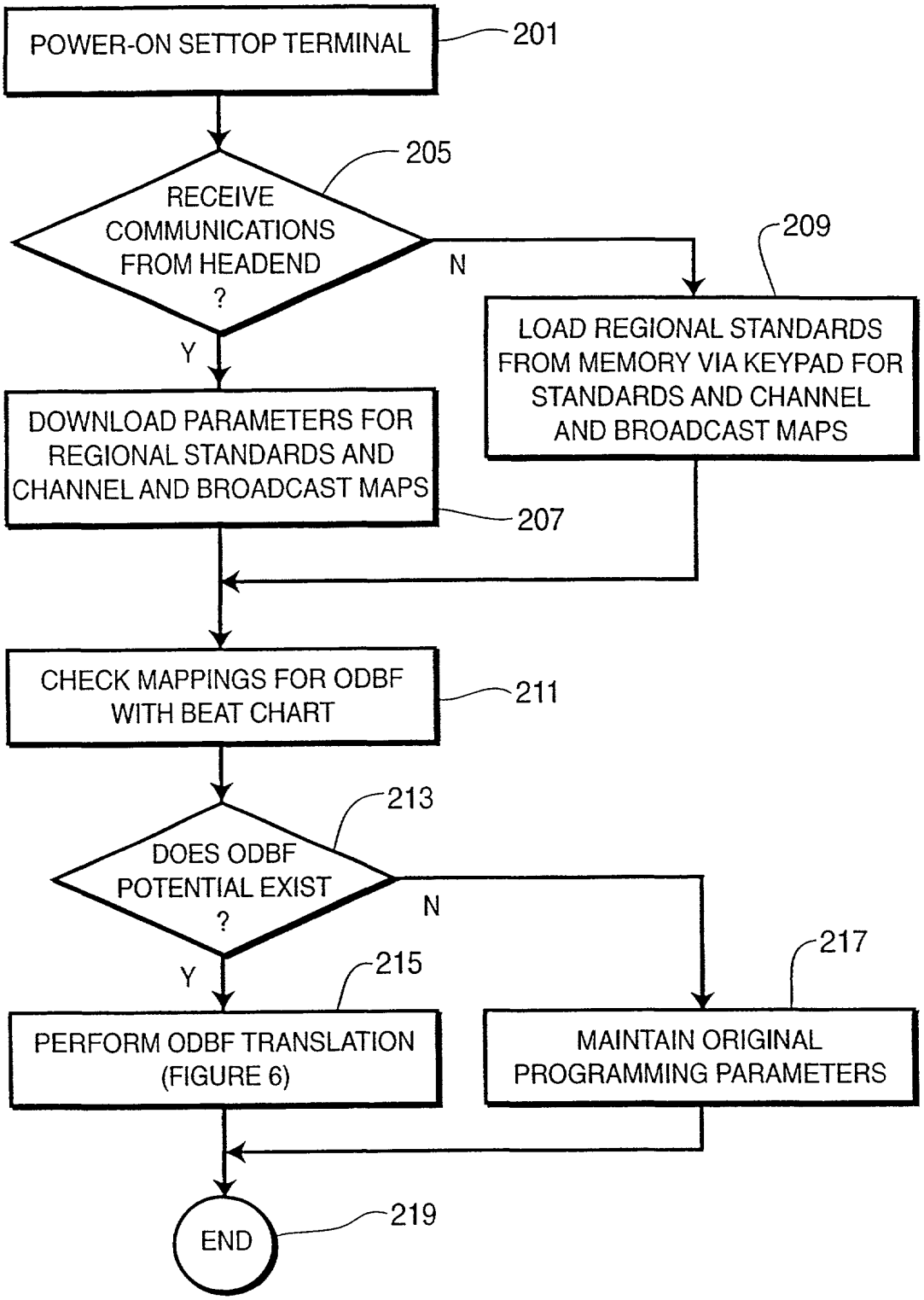
POWER-ON SETTOP TERMINAL
201
RECEIVE COMMUNICATIONS FROM HEADEND ?
205
N
209
Y
LOAD REGIONAL STANDARDS FROM MEMORY VIA KEYPAD FOR STANDARDS AND CHANNEL AND BROADCAST MAPS
DOWNLOAD PARAMETERS FOR REGIONAL STANDARDS AND CHANNEL AND BROADCAST MAPS
207
CHECK MAPPINGS FOR ODBF WITH BEAT CHART
211
DOES ODBF POTENTIAL EXIST ?
213
N
Y
215
217
PERFORM ODBF TRANSLATION (FIGURE 6)
MAINTAIN ORIGINAL PROGRAMMING PARAMETERS
END
219

FIG. 5

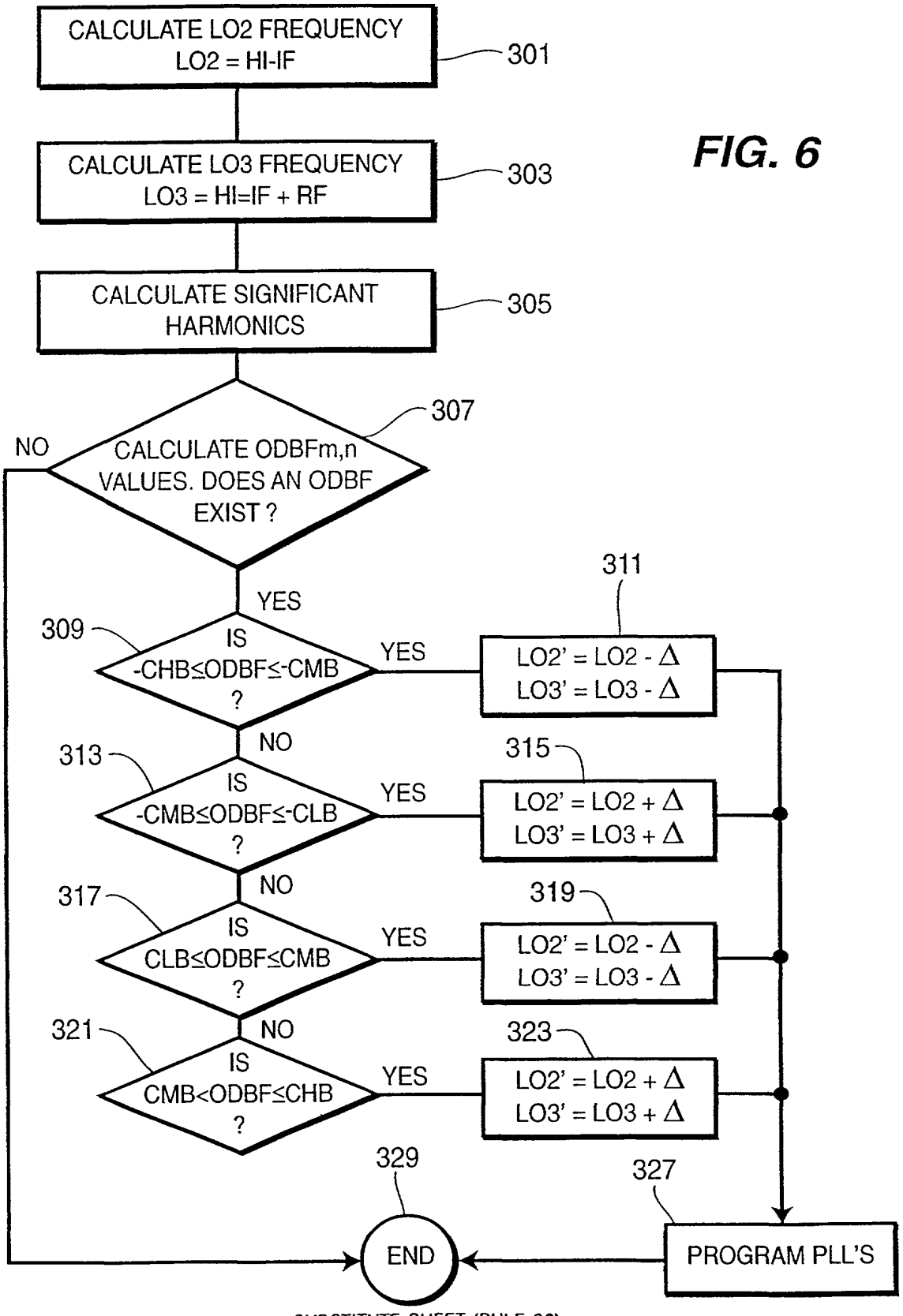
CALCULATE LO2 FREQUENCY
LO2 = HI-IF
301
CALCULATE LO3 FREQUENCY
LO3 = HI=IF + RF
303
CALCULATE SIGNIFICANT HARMONICS
305
307
CALCULATE ODBFm,n VALUES. DOES AN ODBF EXIST ?
NO
YES
309
IS -CHB≤ODBF≤-CMB ?
YES
311
LO2' = LO2 - Δ
LO3' = LO3 - Δ
NO
313
IS -CMB≤ODBF≤-CLB ?
YES
315
LO2' = LO2 + Δ
LO3' = LO3 + Δ
NO
317
IS CLB≤ODBF≤CMB ?
YES
319
LO2' = LO2 - Δ
LO3' = LO3 - Δ
NO
321
IS CMB<ODBF≤CHB ?
YES
323
LO2' = LO2 + Δ
LO3' = LO3 + Δ
329
END
327
PROGRAM PLL'S

FIG. 6

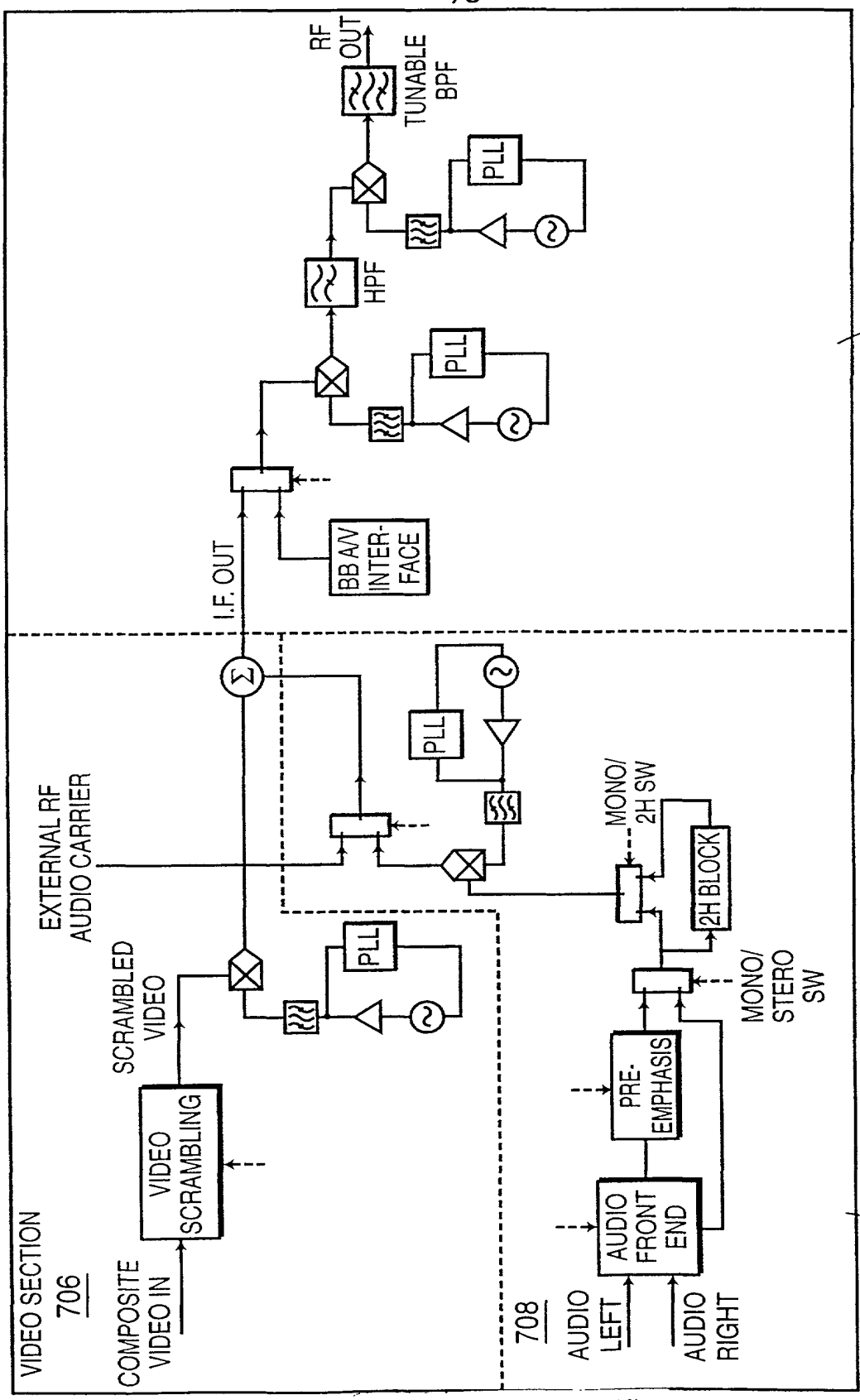

FIG. 7
PRIOR ART

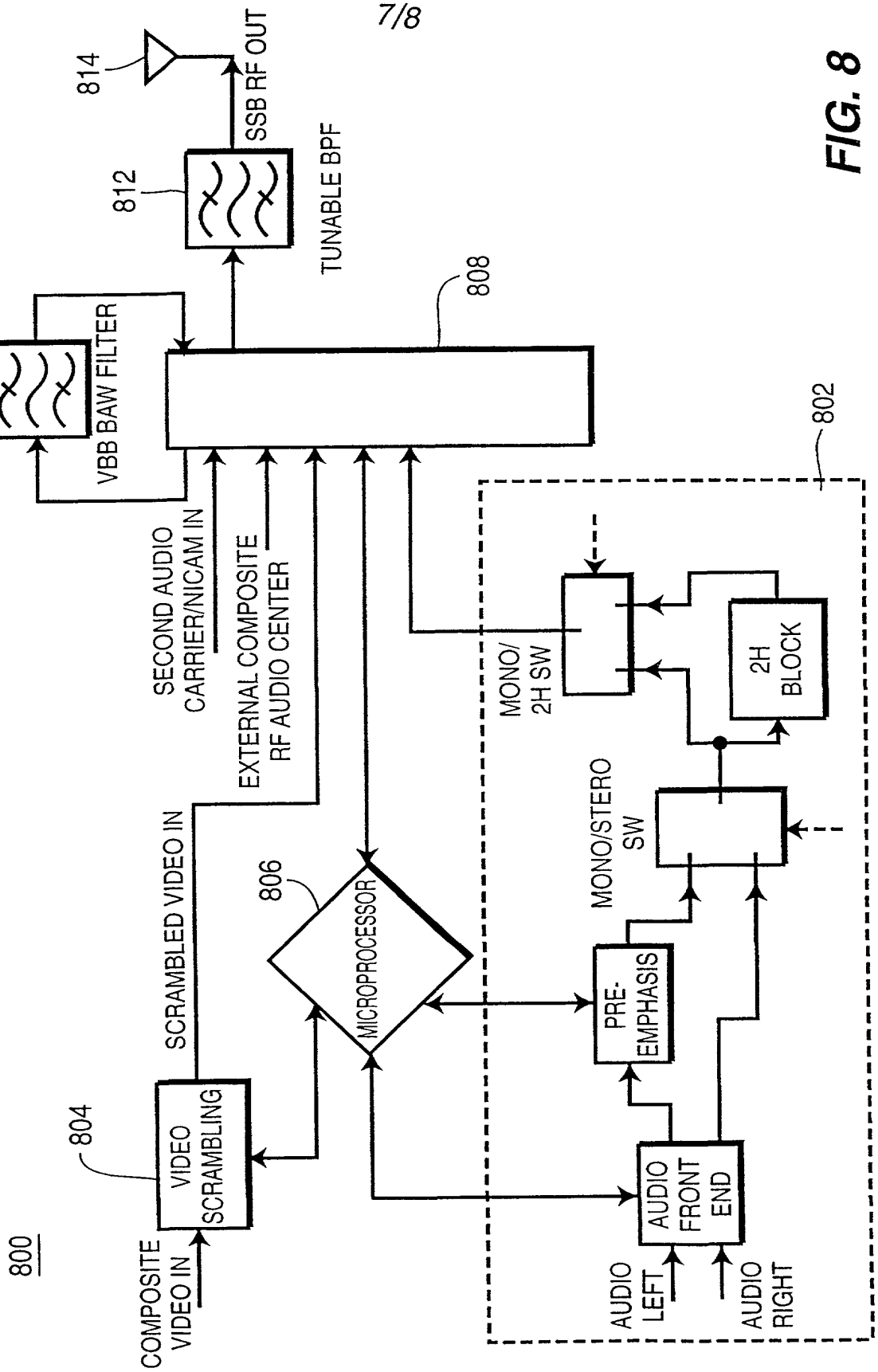
800
802
804
806
808
810
812
814
COMPOSITE VIDEO IN
VIDEO SCRAMBLING
SCRAMBLED VIDEO IN
MICROPROCESSOR
EXTERNAL COMPOSITE RF AUDIO CENTER
SECOND AUDIO CARRIER/NICAM IN
VBB BAW FILTER
TUNABLE BPF
SSB RF OUT
AUDIO LEFT
AUDIO RIGHT
AUDIO FRONT END
PRE-EMPHASIS
MONO/STERO SW
MONO/ 2H SW
2H BLOCK

FIG. 8

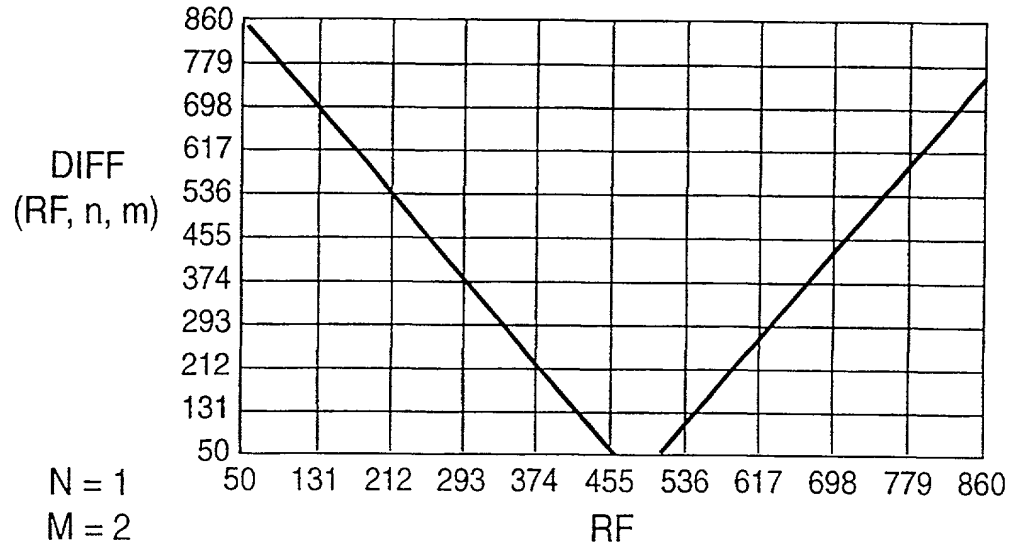
DIFF
(RF, n, m)
860
779
698
617
536
455
374
293
212
131
50
50 131 212 293 374 455 536 617 698 779 860
RF
N = 1
M = 2

FIG. 9A

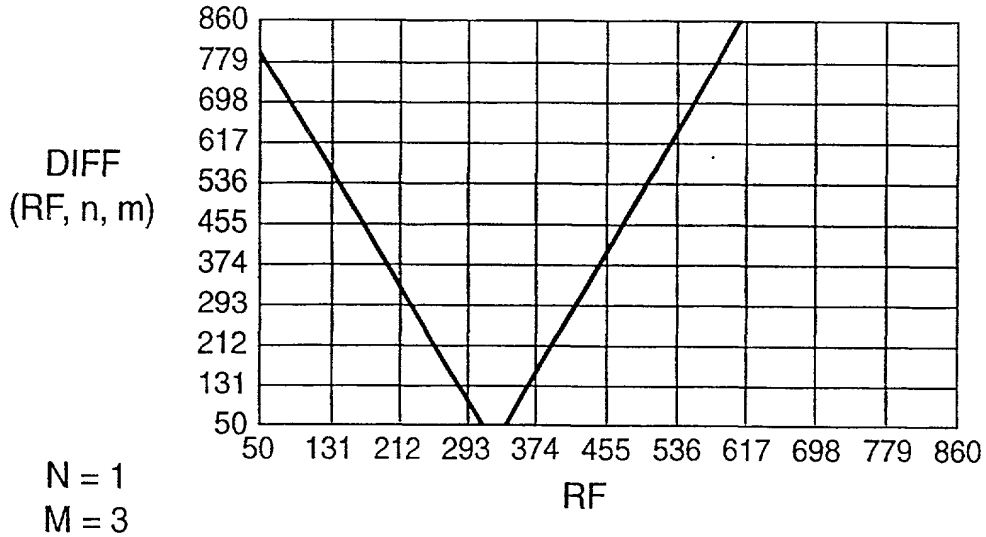
DIFF
(RF, n, m)
860
779
698
617
536
455
374
293
212
131
50
50 131 212 293 374 455 536 617 698 779 860
RF
N = 1
M = 3

FIG. 9B

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[X] Declaration Submitted with Initial Filing OR [ ] Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	MOT-D2174
First Named Inventor	Waight et al.
COMPLETE IF KNOWN	
Application Number	
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

UNIVERSAL MODULATOR

(Title of the Invention)

the specification of which
[X] is attached hereto
OR
[ ] was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]

[ ] Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	
60/110,254	11/30/1998	[ ] Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number *(if applicable)*
PCT/US99/28232	11/30/1999	

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☒ Customer Number 24375 → *Place Customer Number Bar Code Label here*
OR
☐ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number
Namely, the Attorneys of Volpe and Koenig, P.C.			

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☒ Customer Number or Bar Code Label 24375 *OR* ☐ Correspondence address below

Name	VOLPE AND KOENIG, P.C. DEPT MOT				
Address					
Address					
City		State		ZIP	
Country		Telephone		Fax	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Matthew G.	Waight

Inventor's Signature	Matthew G. Waight					Date	5/24/01
Residence: City	Pipersville	State	PA	Country	USA	Citizenship	USA
Post Office Address	2982 E. Rolling Glen Drive						
Post Office Address							
City	Pipersville	State	PA	ZIP	18947	Country	USA

☒ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

1-a

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet
Page 1 of 1

2-00

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any])	Family Name or Surname		
Dipakkumar R.	Patel		
Inventor's Signature D. R. Patel			**Date** 5/22/01
Residence: City Hatboro	**State** PA	**Country** USA USX	**Citizenship** USA
Mailing Address 227 E. Montgomery Avenue			
Mailing Address			
City Hatboro	**State** PA	**ZIP** 19040	**Country** USA

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any])	Family Name or Surname		
Inventor's Signature			**Date**
Residence: City	**State**	**Country**	**Citizenship**
Mailing Address			
Mailing Address			
City	**State**	**ZIP**	**Country**

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any])	Family Name or Surname		
Inventor's Signature			**Date**
Residence: City	**State**	**Country**	**Citizenship**
Mailing Address			
Mailing Address			
City	**State**	**ZIP**	**Country**

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